

BUFFER CIRCUIT DEVICE SUPPLYING A COMMON MODE VOLTAGE  
APPLICABLE TO A NEXT-STAGE CIRCUIT RECEIVING OUTPUT  
SIGNALS OF THE BUFFER CIRCUIT DEVICE

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CROSS REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-336794, filed on November 20, 2002, the entire contents of which are incorporated herein by reference.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a signal transmission technique for transmitting signals at high speed between LSI chips or between elements or circuit blocks in an LSI chip, and between circuit boards or cabinets. More particularly, the present invention relates to a buffer circuit device for distributing a high-speed clock signal or outputting a high-speed data signal.

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2. Description of the Related Art

Recently, the performance of components used in computers and other information processing apparatuses has been greatly improved. In particular, dramatic improvements have been made, for example, in the performance of semiconductor memory devices such as SRAMs (Static Random Access Memories) and DRAMs (Dynamic Random Access Memories), and other semiconductor devices such as processors and switching LSIs. The improvements in the performance of semiconductor memory devices, processors, and the like have reached the point where system performance cannot be improved further unless the speed of signal transmission between components or elements is increased.

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Specifically, the speed gap between a DRAM and a processor (i.e., between LSIs), for example, has been

widening year by year and, in recent years, this speed gap has been becoming a bottleneck impeding performance improvement for a computer as a whole. Furthermore, with increasing integration and increasing size of semiconductor chips, the speed of signal transmission between elements or circuit blocks within a chip is becoming a major factor limiting the performance of the chip. Moreover, the speed of signal transmission between a peripheral device and the processor/chipset is also becoming a factor limiting the overall performance of the system.

By the way, various kinds of clock, data, and the like signals are output through a buffer (buffer circuit device) so as to be transmitted between circuit blocks or LSI chips or cabinets. Especially, differential signals have been transmitted through a differential buffer along with high-speed and low voltage (small signal amplitude) in recent years. However, the common mode voltage of the differential signals output from the buffer and the common mode voltage necessary for a circuit (next-stage circuit) receiving the output signals of the buffer are frequently different. In such a case, an input sensitivity of the next-stage circuit may be reduced so that high-speed signal transmission may not be realized.

The prior art and its associated problems will be described in detail later with reference to relevant drawings.

#### SUMMARY OF THE INVENTION

An object of the present invention is to provide a buffer circuit device supplying a common mode voltage applicable to a next-stage circuit receiving output signals of the buffer circuit device, and to realize a high-speed signal transmission without causing the reduction of an input sensitivity of the next-stage circuit.

According to the present invention, there is

provided a buffer circuit device receiving differential input signals and outputting differential output signals, comprising a buffer circuit receiving the input signals and outputting the output signals; a common mode level  
5 generator circuit outputting a specific level of a common mode voltage for the output signals to be output from the buffer circuit; a common mode voltage detection circuit detecting a common mode voltage of specific signals; and  
10 a bias voltage adjusting circuit adjusting a bias voltage to be supplied to the buffer circuit by comparing an output signal of the common mode level generator circuit with an output signal of the common mode voltage detection circuit.

The common mode level generator circuit may output a  
15 signal having a preferable voltage level as a common mode voltage of input signals of a next-stage circuit to which the output signals of the buffer circuit are supplied. The common mode voltage detection circuit may detect a common mode voltage of the output signals of the buffer  
20 circuit. The common mode voltage detection circuit may detect a common mode voltage of output signals of the next-stage circuit.

The common mode voltage detection circuit may output the output signal to the bias voltage adjusting circuit  
25 by processing the detected common mode voltage and an output voltage of the common mode level generator circuit. The common mode voltage detection circuit may comprise first and second resistor elements coupling the differential input signals; and a third resistor element  
30 connected in series to an output of the common mode level generator circuit.

The common mode voltage detection circuit may further comprise a first capacitor element connected  
35 between a common connection node of the first and second resistor elements and a specific power supply line; and a second capacitor element connected between an output node of the third resistor element and the specific power

supply line. The bias voltage adjusting circuit may be a comparator having a first input connected to the common connection node of the first and second resistor elements and a second input connected to the output node of the  
5 third resistor element.

The common mode level generator circuit may comprise a replica circuit depending on the next-stage circuit. The replica circuit may have features corresponding to all the features of the next-stage circuit. The replica  
10 circuit may have features corresponding to some features of the next-stage circuit.

The common mode level generator circuit may comprise a constant current source. The common mode level generator circuit may comprise a plurality of resistor  
15 elements connected between a high potential power supply line and a low potential power supply line, and may generate a specific level divided by the plurality of resistor elements.

#### BRIEF DESCRIPTION OF THE DRAWINGS

20 The present invention will be more clearly understood from the description of the preferred embodiments as set forth below with reference to the accompanying drawings, wherein:

Fig. 1 is a circuit diagram showing one example  
25 of a buffer circuit device according to the prior art;

Fig. 2 is a circuit diagram showing the basic configuration of a buffer circuit device according to the present invention;

Fig. 3 is a circuit diagram showing a first  
30 embodiment of the buffer circuit device according to the present invention;

Fig. 4 is a circuit diagram showing a second embodiment of the buffer circuit device according to the present invention;

35 Fig. 5 is a circuit diagram showing a third embodiment of the buffer circuit device according to the present invention;

Fig. 6 is a block diagram schematically showing a fourth embodiment of the buffer circuit device according to the present invention;

Fig. 7 is a block diagram schematically showing a fifth embodiment of the buffer circuit device according to the present invention; and

Fig. 8 is a block diagram schematically showing a sixth embodiment of the buffer circuit device according to the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before proceeding to the detailed description of a buffer circuit device according to the present invention, a prior art buffer circuit device and its associated problems will be described with reference to Fig. 1.

Figure 1 shows one example of a buffer circuit device according to the prior art and, more particularly, shows a buffer circuit based on differential CML (Current Mode Logic).

As shown in Fig. 1, the prior art buffer circuit device comprises loads 101, 102 connected to a high potential power supply line Vdd; n-channel type MOS transistors (nMOS transistors) 103, 104 whose gates receive differential (complementary) input signals in, /in and whose drains are connected to the loads 101, 102; and an nMOS transistor 105 connected between sources of the nMOS transistors 103, 104 and a low potential power supply line Vss, whose gate receives a bias voltage bias. Here, differential output signals out and /out are output from a connection node N101 of the load 102 and the drain of the nMOS transistor 104 and a connection node N102 of the load 101 and the drain of the nMOS transistor 103, respectively.

By the way, in recent years, the power supply voltage (Vdd) applied to the above described buffer circuit device is, for example, 1.2 V or lower, and a common mode voltage (center voltage between a voltage of a high level "H" and a voltage of a low level "L" of

output signals) is, generally determined to be a voltage higher than  $V_{dd}/2$  (for example, 0.8 V when the power supply voltage ( $V_{dd}$ ) is 1.2 V).

5 In the prior art, there is proposed a receiver circuit used for a signal transmission system to realize a high accuracy signal transmission (high accuracy signal detection) by effectively controlling a common mode voltage. The receiver circuit has a capacitor network portion receiving differential input signals and a  
10 comparator portion, and maintains the common mode voltage at about a constant value. This prior art receiver circuit is, for example, disclosed in Japanese Unexamined Patent Publication No. 2000-196680 (corresponding to U.S. Patent Nos. 6,166,971 and 6,400,616, and EP-0963083-A2).

15 In recent years, for example, a high speed signal transmission carried out in an LSI is generally designed by using a buffer circuit based on differential CML, and a common mode voltage of output signals is generally higher than a voltage of  $V_{dd}/2$ . On the other hand, a  
20 next-stage circuit receiving the output signals of the buffer circuit requires an individual common mode voltage (in many cases,  $V_{dd}/2$ ) of input signals in accordance with the circuit features thereof and, therefore, an input sensitivity of the next-stage circuit is reduced  
25 when the buffer circuit outputs output signals having a common mode voltage which is not applicable to the next-stage circuit. This problem of the buffer circuit not only appears in a clock buffer circuit used for distributing a clock signal, but it also appears in  
30 other general buffer circuits (general buffer circuit devices) used for buffering various signals.

Next, the basic configuration of a buffer circuit device according to the present invention will be described.

35 Figure 2 shows the basic configuration of a buffer circuit device according to the present invention.

As shown in Fig. 2, a buffer circuit 11 receives

input signals IN, /IN and outputs output signals OUT, /OUT, and a level generator circuit (common mode level generator circuit) 12 generates a specific level common mode voltage of the output signals OUT, /OUT output from the buffer circuit 11. Further, a common mode detection circuit (common mode voltage detection circuit) 13 detects a common mode voltage of specific signals such as the output signals of the buffer circuit 12 or output signals of a next-stage circuit 2, and a bias adjusting circuit 14 adjusts a bias voltage BIAS which is supplied to the buffer circuit 11 by comparing the output of the common mode level generator circuit 12 and the output of the common mode voltage detection circuit 13.

In this way, a common mode voltage of the output signals OUT, /OUT output from the buffer circuit device 1 to the next-stage circuit 2 is applicable to the next-stage circuit 2 and, thereby, the next-stage circuit (receiver circuit) 2 receives the output signals OUT, /OUT of the buffer circuit device having the common mode voltage applicable to the next-stage circuit 2 without causing a deterioration of the input sensitivity thereof.

Below, embodiments of the buffer circuit device according to the present invention will be described in detail with reference to the accompanying drawings.

Figure 3 shows a first embodiment of the buffer circuit device according to the present invention. In Fig. 3, reference numeral 1 denotes a buffer circuit device, 11 denotes a buffer circuit, 12 denotes a common mode level generator circuit, 13 denotes a common mode voltage detection circuit, 14 denotes a bias adjusting circuit, and 2 denotes a next-stage circuit. Further, reference IN, /IN denote differential input signals, OUT, /OUT denote differential output signals, Vdd denotes a high potential power supply line (high potential power supply voltage), and Vss denotes a low potential power supply line (low potential power supply voltage).

As shown in Fig. 3, in the first embodiment of the

buffer circuit device according to the present invention, the buffer circuit 11 is constituted by a buffer (buffer circuit) based on differential CML, which is similar to that described above with reference to Fig. 1.

5 Specifically, the buffer circuit 11 comprises loads 111, 112 connected to the high potential power supply line Vdd; nMOS transistors 113, 114 whose gates receive differential (complementary) input signals IN, /IN and whose drains are connected to the loads 111, 112; and an  
10 nMOS transistor 115 connected between sources of the nMOS transistors 113, 114 and the low potential power supply line Vss, whose gate receives a bias voltage BIAS (output of the bias adjusting circuit 14). Here, differential output signals OUT and /OUT are output from a connection  
15 node N1 of the load 112 and a drain of the nMOS transistor 114 and a connection node N2 of the load 111 and a drain of the nMOS transistor 113, respectively.

In the first embodiment of the buffer circuit device according to the present invention, the common mode level generator circuit 12 comprises a replica circuit having a  
20 construction corresponding to the next-stage circuit 2. Specifically, the next-stage circuit 2 comprises pMOS transistors 21, 22 and 23, 24 used for loads, nMOS transistors 25, 26 used for differential input  
25 transistors, and an nMOS transistor 27 whose gate receives a constant voltage (bias voltage) Vcn. Similarly, the common mode level generator circuit (replica circuit) 12 comprises pMOS transistors 121, 122 and 123, 124, nMOS transistors 125, 126, and an nMOS  
30 transistor 127 whose gate receives the constant voltage (bias voltage) Vcn. Here, in the common mode level generator circuit (replica circuit) 12, input terminals (differential input terminals) and output terminals (differential output nodes) are short-circuited, as the  
35 common mode level generator circuit 12 is only used to generate the common mode voltage.

The common mode voltage detection circuit 13 couples



the differential output signals OUT, /OUT of the buffer circuit 11 by using resistor elements 132, 131, an output signal of the common mode voltage detection circuit 13 (signal at a common node of the resistor elements 131 and 132) is supplied to a positive logic input terminal of the bias adjusting circuit (comparator) 14, and an output signal of the common mode level generator circuit 12 is applied to a negative logic input terminal of the bias adjusting circuit 14 through a resistor element 133.

Here, capacitor elements 135 and 134 are provided between the positive and negative input terminals of the bias adjusting circuit 14 and the low potential power supply line Vss. Further, the differential output signals OUT, /OUT of the buffer circuit 11 are supplied to the next-stage circuit 2 as differential input signals thereof.

As described above, an output signal (bias voltage BIAS) of the bias adjusting circuit (comparator) 14 is fed back to the gate of nMOS transistor 115 of the buffer circuit 11 and, thereby, the common mode voltage of the output signals (OUT, /OUT) of the buffer circuit 11 is adjusted to fit with a level of the common mode voltage of the next-stage circuit 2.

In this way, according to the first embodiment of the buffer circuit device of the present invention, a replica circuit of the next-stage circuit 2 is used as the common mode level generator circuit 12, and therefore, the output signals OUT, /OUT having a common mode voltage to maximize a gain of the next-stage circuit 2 can be output.

Figure 4 shows a second embodiment of the buffer circuit device according to the present invention.

As it is clear by comparing Fig. 4 with the above explained Fig. 3, in the buffer circuit device 1 of the second embodiment of the present invention, the common mode level generator circuit 12 does not correspond all the features of the next-stage circuit 2, and corresponds to only a some features (features for one of the

differential signals) of the next-stage circuit 2. Specifically, in the second embodiment of the buffer circuit device according to the present invention, the common mode level generator circuit (replica circuit) 12  
5 is constituted by pMOS transistors 121', 122' and nMOS transistors 125', 127'. Here, the nMOS transistor 127' of the common mode level generator circuit 12 has a half size of the nMOS transistor 127 of the common mode level generator circuit 12 of the first embodiment shown in  
10 Fig. 3, that is, a gate width of the transistor 127' is a half size of that of the transistor 127.

Figure 5 shows a third embodiment of the buffer circuit device according to the present invention.

As shown in Fig. 5, in the buffer circuit device 1  
15 of the third embodiment according to the present invention, the next-stage circuit 2 comprises two inverters (transistors 201, 202; 203, 204) to amplify the differential output signals OUT, /OUT of the buffer circuit 11 (buffer circuit device 1), and further, the  
20 common mode level generator circuit (replica circuit) 12 is also constituted by an inverter having a pMOS transistor 1201 and an nMOS transistor 1202.

As described above, the features of the common mode level generator circuit 12 can be modified in accordance  
25 with that of the next-stage circuit 2 and, thereby, a common mode voltage of the output signals of the buffer circuit device 1 can be generated to suit the next-stage circuit 2.

Figure 6 schematically shows a fourth embodiment of  
30 the buffer circuit device according to the present invention.

As shown in Fig. 6, in the fourth embodiment of the buffer circuit device according to the present invention, the common mode level generator circuit 12 is constituted  
35 by a constant current source. Here, the other features of the buffer circuit device of the fourth embodiment, that is, the features of the buffer circuit 11, the

common mode voltage detection circuit 13 and the bias adjusting circuit 14 are, for example, the same as that described in the first embodiment with reference to Fig. 3.

5           In the buffer circuit device of the fourth embodiment according to the present invention, a constant current source is used as the common mode level generator circuit 12 and, therefore, output signals OUT, /OUT having a common mode voltage not receiving the influence  
10 of fluctuations of the power supply voltage or circumstance temperature, can be output. The buffer circuit device of the fourth embodiment is suitable for the case when a signal level range of the input signals of the next-stage circuit 2 (differential output signals  
15 OUT, /OUT of the buffer circuit device) is previously determined, wherein the differential output signals OUT, /OUT can be controlled within the specific signal level range. Here, various types of known constant current sources can be applied as the constant current source of  
20 the common mode level generator circuit 12.

Figure 7 schematically shows a fifth embodiment of the buffer circuit device according to the present invention.

25           As it is clear by comparing Fig. 7 with the above explained Fig. 6, in the buffer circuit device 1 of the fifth embodiment according to the present invention, the common mode detection circuit 13 receives output signals (differential output signals) of the next-stage circuit 2 and the level of the bias signal BIAS output from the  
30 bias adjusting circuit 14 is controlled in accordance with the output signals of the next-stage circuit 2.

          According to the buffer circuit device of the fifth embodiment of the present invention, for example, the differential output signals of the next-stage circuit 2  
35 can be controlled within a predetermined level range.

Figure 8 schematically shows a sixth embodiment of the buffer circuit device according to the present

invention.

As shown in Fig. 8, in the buffer circuit device of the sixth embodiment according to the present invention, the common mode level generator circuit 12 is constituted by resistor elements 12a, 12b connected between the high potential power supply line Vdd and the low potential power supply line Vss, and a voltage divided by the resistor elements 12a, 12b is supplied to the common mode voltage detection circuit 13 as an output of the common mode level generator circuit 12.

According to the buffer circuit device of the sixth embodiment of the present invention, an output of the common mode level generator circuit 12 is generated by dividing the power supply voltage using resistor elements and, therefore, a feedback control can be carried out without receiving the influence of fluctuations of the power supply voltage or temperature. Here, the resistor elements 12a, 12b are, for example, made of poly-silicon.

As described above, according to a buffer circuit device of the present invention, a common mode voltage applicable to a next-stage circuit receiving output signals of the buffer circuit device can be generated and, therefore, a high-speed signal transmission can be realized without causing the reduction of an input sensitivity of the next-stage circuit.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.